THE REMARKS

Claims 1-23 were pending prior to entering the amendments.

The Amendments

Independent claims 1 and 11 have been amended. Dependent claims 2-3 and 14 and 15 have been amended. Claim 23 is canceled. Claim 24-26 is a new claim. Support for these amendments and the new claims is as follows:

Claim 1 – Fig. 18, Fig. 49, page 29, lines 22-30, page 30, lines 1-2, page 46, and lines 18-28; page 44, lines 19-25, page 2, lines 2-23.

Claim 11 – Same as claim 1, plus Fig. 52, page 46, lines 20-21, and page 48, lines 7-15.

Claims 2-3, 14-15 - page 44, lines 26-28.

Claims 24 – Fig. 18, Fig. 49, page 29, lines 22-30, page 30, lines 1-2, page 46, and lines 18-28.

Claims 25-26 - page 41, lines 6-7 and lines 12-18, and Fig. 48, page 42, lines 10-19.

No new matter is introduced in any of the above amendments. The Examiner is requested to enter the amendment and re-consider the application.

35 U.S.C. §103(a) Rejection

Claims 1-11 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Navada, et al., hereinafter Navada (US2003/0214956) in view of Krishnan (US2003/00225907).

Note: In the office action dated 8/19/2008, the Examiner did not provide a statement for a basis of rejection for claims 12-13. The Examiner is requested to provide such a statement. Additionally, for claims 14-23, there were individual statements for the claim rejections, but there was not a general statement related to the sources for rejection. The applicant assumed that the above statement applies to claims 14-23 (i.e. over Navada in view of Krishnan).

In response, claim 1 has been amended. Amended claim 1 recites:

> A processor readable medium encoding a data structure for supporting one or more packet modification operations, the data structure comprising:
>
> a first pointer to a sequence of one or more commands, for execution by a processor, implementing one or more packet modification operations and

stored in a first memory area; and

a second pointer to a burst of one or more data or mask items for use by the processor in executing the one or more commands stored in a second memory area distinct from the first;

wherein the data structure is located in a third memory and the data structure is accessed via a data structure index, wherein the data structure index is embedded in the one or more packets;

wherein data is selectively shifted and masked in each of plurality of categories responsive to the one or more decoded commands, thereby performing one or more packet modification operations in the packet;

wherein the selectively shifted and masked data is logically summed into the plurality of categories.

Neither Navada nor Krishnan teach a data structure having the elements illustrated in Fig. 49, with multiple pointers, and implementing a plurality of commands, the shift and mask functionalities, and logical summation.

The Applicant's support for this amendment is Fig. 18, Fig. 49, page 29, lines 22-30, page 30, lines 1-2, page 46, and lines 18-28; page 44, lines 19-25, page 2, lines 2-23. Per this citation, "the data structure 4904 comprises a pointer 4906 to a sequence 4910 of one or more commands implementing one or more packet modification operations and stored in a first memory area 4912, and a pointer 4908 to a burst 4914 of one or more data or mask items for use by the one or more commands and stored in a second memory area 4916 distinct from the first." As described, the first pointer is coupled only to the first memory area and the second pointer is only coupled to the second memory area.

Relative to Navada, Navada describes a system for efficient fast VLAN lookups and inserts as illustrated in Navada Fig. 2. In Fig. 2, a pointer table is illustrated, 205, along with a data entry table, 203. Navada's system functions by accessing pointers within table 205 that "point" to a appropriate data entry memory cell in table 203.

This structure compares with the Applicant's structure in Fig. 49. In that structure, the processor readable medium 4902 comprises multiple pointers, but these pointers access separate distinct memories for separate functional purposes, i.e. accesses a sequence of commands or accessing a burst of one or more data or mask items. Further, this combination of activities (commands and burst of data/masks) results in packet modification. Navada does note that

pointers and data can be stored in different memory arrangements (Navada [0026]), Navada does not teach this specific data structure and the associated functionality the data structure provides. This functionality includes the selective shifting of data and logically summing data which is not disclosed by Navada.

Relative to Krishnan, Krishnan describes packet modification operations, but only as a general concept of inserting bits in a packet. Krishnan does not describe the selective shifting of data and logically summing data as part of the process.

Therefore, these elements of claim 1 are not described by Navada or Krishnan, considered singly or in combination. Accordingly, the Applicant respectfully asserts that amended claim 1 is an allowable claim.

Independent Claim 11

Amended Claim 11 is a method claim with similar elements as amended claim 1. Hence, the aforementioned comments provided for claim 1 also apply to claim 11. Additionally, claim 11 recites the following elements:

> performing packet classification while the packet is located within a first portion of a switch;
>
> inserting a data structure index in the packet while the packet is located within a second portion of the switch;

These elements are supported in the Applicant's Specification: Fig. 52, page 46, lines 20-21, and page 48, lines 7-15. Neither Navada nor Krishnan disclose these concepts considered singly or in combination. Accordingly, the Applicant respectfully asserts that amended claim 11 is allowable claim.

Dependent Claims 2-10 and 11-22

Claims 2-10 and 11-22 are directly or indirectly dependent on amended claims 1 or 11. The Applicant respectfully asserts that claims 2-10 and 11-22 are allowable at least based on an allowable base claim.

In addition, the applicant provides the following arguments and comments:

Dependent claims 2-3, and 14-15 have been amended and these claims describe different methods for generating a data structure described in the Applicant's inventions. The methods include, "generated during receive-side classifications processing of a packet", and "generated by a host CPU coupled to a switch fabric". These claims are supported in the Applicant's Specification, page 44, lines 26-28. Neither Navada nor Krishnan teach these concepts considered singly or in combination. Accordingly, the Applicant respectfully asserts that amended claims 2-3 and 14-15 are allowable claims.

New Claims

Independent Claim 24 and Dependent Claim 27.

Independent claim 24 describes a pipeline processor core comprising several key elements of the applicant's invention:

> A pipeline processor core comprising:
>
> a data structure comprising two or more pointers;
>
> a command fetch stage configured to fetch one or more commands obtained using a first pointer to access a first memory;
>
> a command decode stage configured to decode the one or more commands;
>
> an address and mask generation stage configured to generate one or more addresses and one or more mask for each of the commands;
>
> a data shift, mask and sum stage wherein packet data is selectively shifted and masked in each of plurality of categories in response to a decoded command, wherein data shifting and masking is based upon a burst of one or more data and mask items obtained using a second pointer to access a second memory which is distinct from the first memory;
>
> wherein the pipeline processor core supports a data structure comprising two or more pointers;
>
> wherein the first and second pointers are located in the data structure that is accessed from a third memory via a data structure index, wherein the data structure index is embedded in one or more data packets;
>
> wherein the selectively shifted and masked data is logically summed into the plurality of categories.

The applicants support for this amendment is Fig. 18, Fig. 49, page 29, lines 22-30, page 30, lines 1-2, page 46, lines 18-28.

Neither Navada nor Krishnan describe a pipeline processor that is utilizes to support the data structure described in the Applicant's invention.

The Applicant discloses elements of a pipeline processor that support the data structure of the Applicant's invention. These elements are illustrated in Fig. 18 and describe in pages 29-30. Fig. 49 illustrates the data structure as it is facilitated in the functional elements of Fig. 18.

Navad and Krishnan describe network systems, but do not describe a pipeline processor. Further, they do not describe a data structure that provides the functional results described in the applicants invention. As one example, neither source describes selectively shifting of bits in relation to the packet modification process.

Therefore, these elements of claim 24 are not described by Navada or Krishman, considered singly or in combination. Accordingly, the Applicant respectfully asserts that new claim 1 is an allowable claim.

Claim 27 is directly dependent on amended claims 24. The Applicant respectfully asserts that claim 27 is allowable at least based on an allowable base claim.

Additionally, relative to dependent claim 27, support for this claim is in fig. 18. Neither Navada nor Krishman, considered singly or in combination describe a transmit modification index is coupled to the data shift, mask and sum stage. Accordingly, the Applicant respectfully asserts that new claim 27 is an allowable claim.

Dependent Claims 25 and 26

Claims 25-26 are directly or indirectly dependent on amended claim 1. The Applicant respectfully asserts that claims 25-26 are allowable at least based on an allowable base claim.

Additionally, Dependent Claim 25 describe the categories of processed data (packet data, insertion or replacement data, copy data, and residual packet data). Claim 26 teaches that the plurality of categories support a nested packet format. Support for these claims is at page 41, lines 6-7 and lines 12-18, and Fig. 48, page 42, lines 10-19. Neither Navada nor Krishnan describe a these categories or the nested packet format.

Therefore, these elements of claim 25-26 are not described by Navada or Krishnan, considered singly or in combination. Accordingly, the Applicant respectfully asserts that new claims 25-26 are allowable claims.

CONCLUSION

Applicants believe that the application is now in good and proper condition for allowance. Early notification of allowance is earnestly solicited.

Respectfully submitted,

Date: January 21, 2008

Donald R. Gibson (Reg. No. 59, 564)

HOWREY LLP
2941 Fairview Park Drive, Box 7
Falls Church, VA 22042
Tel: (650) 798-3570
Fax: (650) 798-3600